REMARKS/ARGUMENTS

After the foregoing Amendment, Claims 32, 34, 38, and 40-44 are currently pending in this application. Claims 4, 11, 14-17, 21 and 24 have been withdrawn from consideration as being directed to non-elected subject matter. Claims 1-3, 5-10, 12, 13, 18-20, 22, 23, 25-31, 33, 35-37, and 39 have been canceled without prejudice. Claims 32, 34, and 38 have been amended in order to more distinctly claim subject matter which the Applicants regard as the invention and to overcome matters brought forth by the Examiner. New claims 40-44 have been added to more distinctly claim subject matter which the Applicants regard as the invention. Applicants submit that no new matter has been introduced into the application by these amendments.

Objections to the Specification

The Examiner objected to the specification because on pages 4 and 5 "it is not clear how the negative going edge can prevent from discharging into the receiver". It is clearly stated in page 5, lines 14-17 that when the tracking device "detects a negative going edge, the tracking system prevents the parasitic capacitor from discharging into the input signal thereby preventing distortion". On page 5, lines 18-20 the tracking device is disclosed as comprising a dv/dt analyzer and a charge

pump which together compensate for the effects of the parasitic capacitance on the input signal. Specifically, it is later explained how the discharge is prevented:

> "During the negative edge of the signal (-dv/dt), the voltage instantaneously decreases at terminal 22 which ultimately causes ***the transistor 20 to prevent the voltage level of terminal 24 to be reduced, thereby preventing occurrence of a glitch during the negative going portion of the input signal.***" (Page 6, lines 4-7; Emphasis Added)

In this embodiment above, the transistor 20 prevents the discharge of the parasitic capacitance to the input signal from occurring. How transistor 20 may do this in described on page 6, lines 4-7 wherein it describes that during a negative edge when the voltage at the input decreases, transistor 20 prevents the voltage level of terminal 24 to be reduced. Thus, it prevents the discharge of the parasitic capacitor onto the falling edge input signal by maintaining the voltage level at node 24. Therefor, the withdrawal of the objection to the specification is respectfully requested.

Claim Rejections - 35 USC § 112 2nd ¶

Claims 32, 34, 35, 38, and 39 stand rejected under 35 USC § 112 2nd ¶ as being indefinite. Claim 38 has been amended in order to overcome any ambiguity with regards to the output of the circuit. Claims 35 and 39 have been canceled without prejudice, therefor making the rejection moot.

With respect to claims 32 and 34 the applicant respectfully argues that the use of a charge pump is found both in the drawings and the specification. Fig. 2B, item 11 specifically shows a charge pump coupled to a dv/dt analyzer. These two components are one embodiment of the "tracking system". The use of the dv/dt analyzer and charge pump are described on page 5, lines 18-20. Fig. 2C shows a transistor layer implementation of the dv/dt analyzer and the charge pump. We believe that the Examiner is misinterpreting the meaning of the term charge pump with a specific implementation commonly used in phase locked loops. Broadly put a charge pump can be any circuit, comprising one or more transistors, that compensates for a change in charge in a signal, node, or device.

With respect to compensating for charge during a negative edge, as described above transistor 20 prevents the discharge of the parasitic capacitance to the input signal from occurring by preventing the voltage level of terminal 24 to be reduced (Pg. 6, lines 4-7). Thus, it prevents the discharge of the parasitic capacitor onto the falling edge input signal by maintaining the voltage level at node 24.

Based on the arguments presented above, withdrawal of the 35 USC § 112 2nd ¶ rejection of claims 32, 34, 35, 38, and 39 is respectfully requested.

Claim Rejections - 35 USC § 102(e)

Claim 32 stands rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 5,973,967 to Nguyen et al. (hereinafter "Nguyen"). Nguyen neither teaches nor suggests the present invention. Nguyen's invention is a page buffer to be used in a memory device. Figure 2 shows the circuit implementation of the page buffer. Figure 2 is not a circuit for compensating for parasitic capacitances at an input of a receiving circuit. In the description of the structure and operation of Figure 2 in Column 3, Nguyen describes the circuit as a buffer to be used in memory. Nguyen does not address using the circuit for compensating for parasitic capacitance when a bit is stored or read.

Regarding claim 32, the claim discloses compensating for a parasitic capacitance of a circuit by using a rate of change of voltage detecting circuit and a charge pump. The claim states that for a detected negative edge, the charge pump has a transistor that prevents discharge of the parasitic capacitance onto the input signal. A particular advantage of claim 32 is that one transistor may help to compensate for the negative edge distortion effects. Nguyen does not address detecting a negative edge and compensating for it using a transistor in a charge pump. Therefor Nguyen does not meet the features of the claim.

Claims 40 and 41 are dependent upon claim 32, which the Applicants believe are allowable over the cited prior art of record for the same reasons provided above.

Based on the arguments presented above, withdrawal of the 35 USC § 102(e) rejection of claim 32 is respectfully requested.

Claims 34-36, 38 and 39 stand rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 6,204,654 to Miranda et al. (hereinafter "Miranda"). Claims 35, 36, and 39 have been canceled making the rejection moot.

After the foregoing amendment, the present invention as claimed in 34 describes a parasitic capacitance compensation circuit for high frequency signals having a certain circuit structure comprising four transistors, a capacitor, and a current source. Miranda does not disclose this claimed circuit anywhere in the disclosure. The various implementations shown by Miranda in figures 5, 9, 10, and 11 are far more complex and do not have the particular circuit layout as claimed.

Claims 38 and 42 are dependent upon claim 34, which the Applicants believe are allowable over the cited prior art of record for the same reasons provided above.

Based on the arguments presented above, withdrawal of the 35 USC § 102(e) rejection of claims 34-36, 38 and 39 is respectfully requested.

Newly added claims 43 and 44 are allowable over the cited prior art of record for the same reasons provided above for claim 34. Neither Nguyen nor Miranda discloses the parasitic capacitance compensation circuit as claimed in 43.

Conclusion

If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephone interview will help to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

In view of the foregoing amendment and remarks, Applicants respectfully submit that the present application is in condition for allowance and a notice to that effect is respectfully requested.

Respectfully submitted,

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